Tech Spec for SDXC Host Controller

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1 Introduction

1.1 Overview

This document gives the Technical Specification of the SDXC host controller core. It includes the overall architectural description, brief functional details and interface and register set definitions for the host controller.

1.2 Features

- Supports standard register set for the host controller
- Supports 32 bit AHB LITE synchronous Host interface working at SOC interface frequency.
- 1-bit/4-bit modes of SD/SDIO supported.
- Supports following UHS –I modes of operations.
    - DS – Default speed mode upto 25MHz 3.3V signaling
    - HS – High Speed mode upto 50MHz 3.3V signaling
    - SDR12 – SDR upto 25MHz 1.8V signaling
    - SDR25 – SDR upto 50MHz 1.8V signaling
    - SDR50 – SDR upto 100MHz 1.8V signaling
    - DDR50 – DDR upto 50MHz 1.8V signaling
- One data Transmit FIFO with 32-bit write width and 256 depths.
- One data Receive FIFO with 32-bit read width and 256 depths.
- SDIO Interrupts, Suspend/Resume Operation and SDIO Read Wait Operation are supported.
- Buffers to store the response received.
- Command buffers to store command index and argument.
- Timeout monitoring for response and data operation.
- Card detect and removal monitoring using debouncing logic.
- Supports various clock frequencies such as 25MHz, 50MHz, 100MHz required for SD/ SDIO operations. Operating frequency configurable through registers.
- CRC generation / checking supported for both command and data transactions.
- Compliant with SD specification version 3.0

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
FSM	Finite State machine
LSB	Least Significant Bit/Byte
MSB	Most Significant Bit/Byte
RAM	Random Access Memory
SD Card	Secured Digital Card
SDIO Card	Secured Digital IO Card
SDMA	Simple Direct Memory Access
SDR	Single Data Rate
SDXC	Secured Digital eXtended Capacity
UHS	Ultra High Speed

2 Host Controller Interface

2.1 Logic Symbol

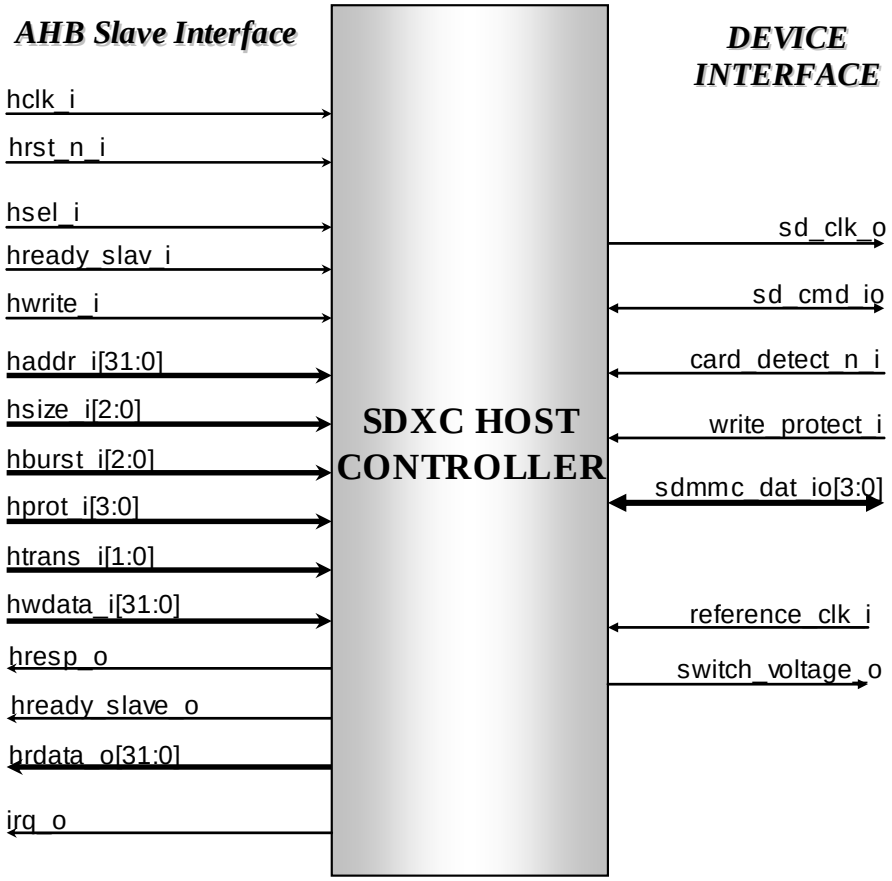

Figure 1 : Host Controller Logic Symbol

2.2 Block Diagram

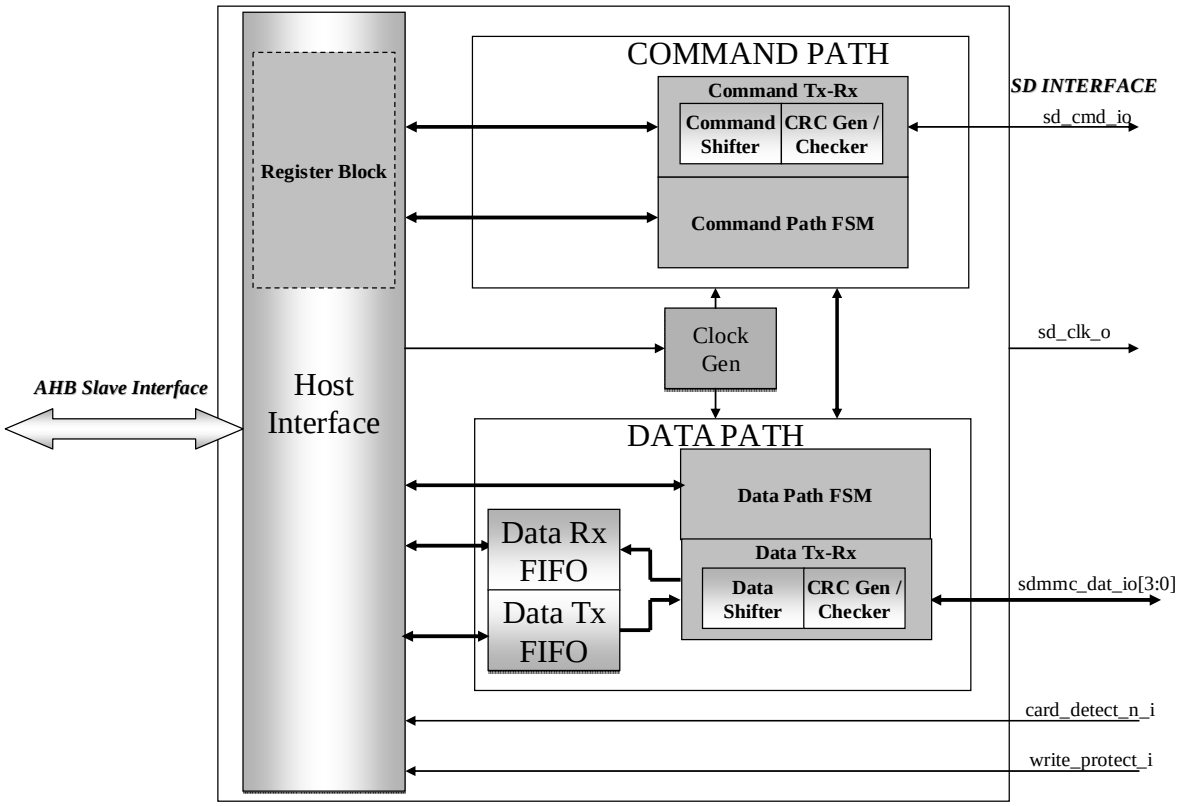

Figure 2: SDXC Host Controller Block Diagram

2.3 Description

- **Host Interface and Register Block**

This module will interface with the AHB master. It consists of a 32 bit register decoder block The Register block has registers used for selecting the controller's mode of operation, clock frequency, Block Length, Number of Blocks, etc. Selective interrupt enabling can be done. The controller will report the internal state machine status, card status and error status to the Processor using Status Registers. The register set is compliant to SD host controller standard Specification version 2.0.

- **Clock Module**

This module will generate and control the different clock frequencies required at different phases of the SD/SDIO operation. Clock frequencies available are 200 KHz, 25 MHz, 50 MHz and 100 MHz.

- **Command Path**

The command path carries out entire command transmission and response reception. This module consists of a command transmitter/receiver; command state machine and 7-bit CRC generator/checker.

- **Data Path**

The data path carries out entire data transmission and reception. This module consists of a data transmitter/receiver, data state machine and 16-bit CRC generator/checker.

- **Tx/Rx FIFOs**

The FIFOs are asynchronous type, and will be capable of storing 1Kbytes of data each. The Processor can write the data to be transmitted in Tx FIFO and receive data in the Rx FIFO.

2.4 I/O Description

The I/O signals of the FPGA are described below.

2.4.1 System Interface Signal Description

Table 2: AHB master interface Signal Description

Signal	I/O	Width	Description
hrst_n_i	I	1	The bus reset input signal is active LOW and resets the system and the bus.
hclk_i	I	1	The bus clock input times all bus transfers. All signal timings are related to the rising edge of hclk_i.
hsel_i	I	1	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave.
haddr_i[31:0]	I	32	The 32-bit system address bus input.
hwrite_i	I	1	Indicates the transfer direction. 1 - Write transfer 0 - Read transfer. It has the same timing as the address signals; however, it must remain constant throughout a burst transfer.

Signal	I/O	Width	Description
hsize_i[2:0]	I	2	Indicates the size of the transfer. 000 - Byte 001 - Half-word 010 - Word. The protocol allows for larger transfer sizes up to a maximum of 1024 bits Others – Not Applicable The current design supports word transfer of data.
hburst_i[2:0]	I	3	The burst type indicates if the transfer is a single transfer or forms part of a burst. 000 – Single Burst Others – Not supported
hprot_i[3:0]	I	4	The protection control signals provide additional information about a bus access and are primarily intended for use by any module that wants to implement some level of protection. 0011 – Corresponds to a non-cacheable, non-bufferable, privileged, data access. Slave interface doesn't use this signal
htrans_i[1:0]	I	2	Indicates the transfer type of the current transfer. The design supports Non Sequential type of transfer. 00 - Idle 01 - Busy 10 – Non Sequential 11 - Sequential.
hready_slav_i	I	1	As an input the from the master, slave interface will sample ahb_sel_i, address and control signals only when this input is HIGH, indicating that current transfer is completing.
hwdata_i[31:0]	I	32	The write data bus is used to transfer data from the master to the slaves during write operations.

Signal	I/O	Width	Description
hready_slav_o	O	1	As an output when HIGH, this signal indicates that a transfer has finished on the bus. This signal driven by slave can be driven LOW to extend a transfer.
hresp_o	O	1	The transfer response output provides the master with additional information on the status of a transfer. 0 - transfer status is OKAY 1 - transfer status is ERROR
hrdata_o[31:0]	O	32	During read operations, the read data output bus transfers data from the slave to the master.

Table 3: SD/SDIO Card Interface Signal Description

SIGNAL NAME	I/O	WIDTH	DESCRIPTION
sd_clk_o	O	1	Clock output to Card
sd_cmd_io	I/O	1	SD/SDIO: Command Line
sd_cmd_dir_o	O	1	Direction control signal towards external buffer for command line
sd_dat_io[0]	I/O	1	SD/SDIO 4-bit Mode: Data line 0 or Busy Status SD/SDIO 1 -bit Mode: Data line or Busy Status
sd_dat_dir_o[0]	O	1	Direction control signal towards external buffer for sd_dat_io[0] line
sd_dat_io[1]	I/O	1	SD/SDIO 4-bit Mode: Data line 1 or SDIO Interrupt line. SDIO 1 -bit mode: SDIO Interrupt line.
sd_dat_dir_o[1]	O	1	Direction control signal towards external buffer for sd_dat_io[1] line
sd_dat_io[2]	I/O	1	SD/SDIO 4-bit Mode: Data line 2 or SDIO Read Wait Signal. SDIO 4-bit Mode: SDIO Read Wait Signal
sd_dat_dir_o[2]	O	1	Direction control signal towards external buffer for sd_dat_io[2] line

sd_dat_io[3]	I/O	1	SD/SDIO 4-bit Mode: Data line 3 SD/SDIO 1 -bit mode: Not used
sd_dat_dir_o[3]	O	1	Direction control signal towards external buffer for sd_dat_io[3] line
card_detect_n_i	I	1	Card Detect from the SD Card Connector
write_protect_i	I	1	Write protect from the SD Card Connector

Table 4: GPIO Signals

SIGNAL NAME	I/O	WIDTH	DESCRIPTION
reference_clock_i	I	1	100MHz Reference clock for SD clock generation
irq_o	O	1	Interrupt pin driven through GPIO pin.
switch_voltage_o	O	1	Switch voltage indicator signal to indicate the external switching circuit to switch operating voltage from 3.3V to 1.8V.(Required for UHS mode of operation during switch command from the Host to the Card)

3 Register Description

3.1 Register List

The IP supports the following 32 bit Register set

Table 5: Register List

Sl.No	Register Name	Description
1.	Block Info Register	This register is used to configure the number of bytes in a data block and to specify the number of data blocks in a block transfer of data.
2.	Command Argument Register	This register contains the SD command argument
3.	Command Register	This register contains the information required for command and data transfer
4.	Response Register0	This register is used to store the response from SD cards
5.	Response Register1	This register is used to store the response from SD cards
6.	Response Register2	This register is used to store the response from SD cards
7.	Response Register3	This register is used to store the response from SD cards
8.	Buffer Data Port Register	This is the 32 bit data port register to access internal buffer
9.	Present state Register	This is a 32 bit Read only register using which the host driver can get the status of the host controller
10.	Host control Register	This register contains the SD command control bit for selecting modes of operation
11.	Clock and Time out control Register	This register specifies the frequency of operation of the SD/SDIO Clock and data time out counter value. The software is responsible for setting this register
12.	Interrupt Status Register	This register specifies the status bits for normal operations start/completion and for error occurrence
13.	Interrupt signal enable Register	This register is used to select which interrupt

		status is notified to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation
14.	Buffer voltage handler	This is the 32 bit register used for the execution of switching command for switching the mode of operation from DS to HS

4 System Implementation

For SDXC operation it is so required that the host controller changes its operating voltage level from 3.3V to 1.8V dynamically. The figure below shows a possible system set up for the same.

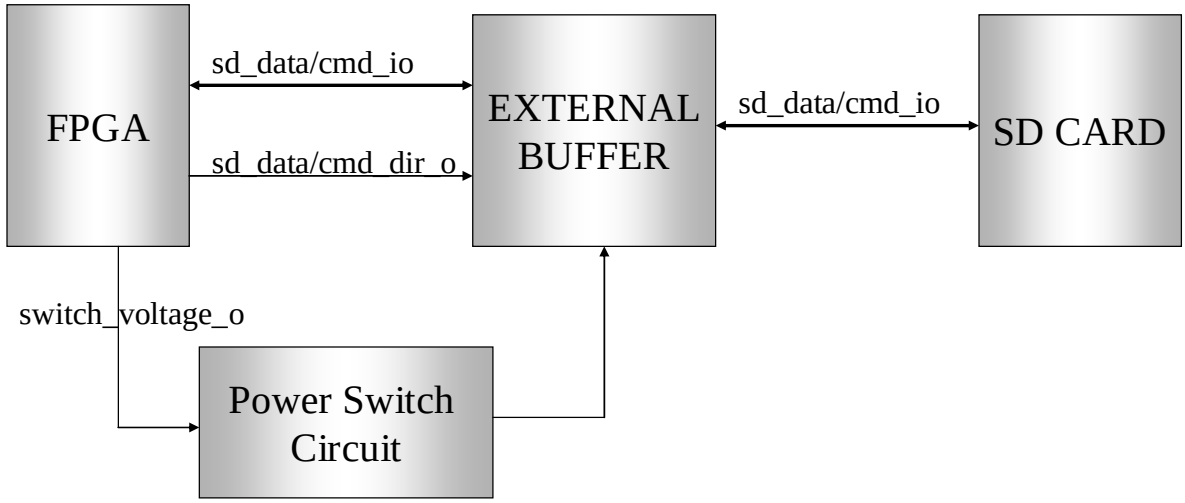

Figure 3: System implementation For Voltage switching

The SDXC specification defines two modes of operation DS i.e. Default speed mode with operating voltage of 3.3V and HS i.e. High speed mode with operating voltage of 1.8V. The system wakes up at DS mode. Whenever the system is required to switch to HS mode then the host controller is required to change its operating voltage level from 3.3V to 1.8V dynamically. To achieve this above set up is used. The blocks perform the following function

- **FPGA**: Drives the bidirectional data and command signals and directional control signal to the External buffer.
- **SD CARD**: Drives the bidirectional data and command signals to the External buffer.
- **EXTERNAL BUFFER**: Depending on the status of sd_data/cmd_dir_o line value controls the direction of the signal driven by FPGA or SD CARD.
- **POWER SWITCH CIRCUIT**: Switches the voltage from 3.3V to 1.8V depending on the status of switch_voltage_o signal.

5 Waveforms

5.1 AHB Slave Interface

5.1.1 Write Cycle

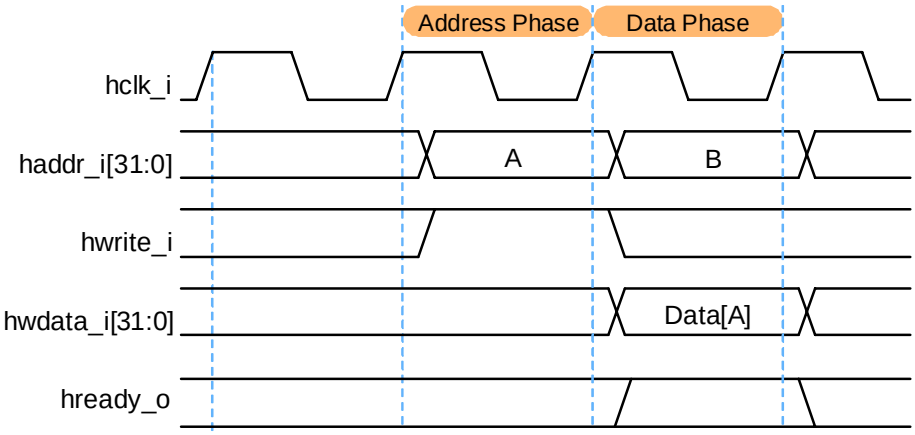

Figure 4: AHB Slave Interface Write Cycle Timing Diagram

5.1.2 Read Cycle

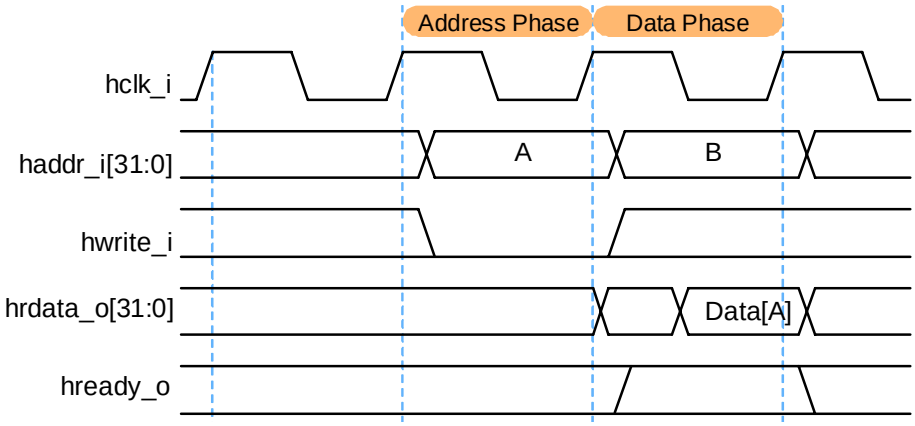

Figure 5: AHB Slave Interface Read Cycle Timing Diagram

5.1.3 Burst Write Cycle

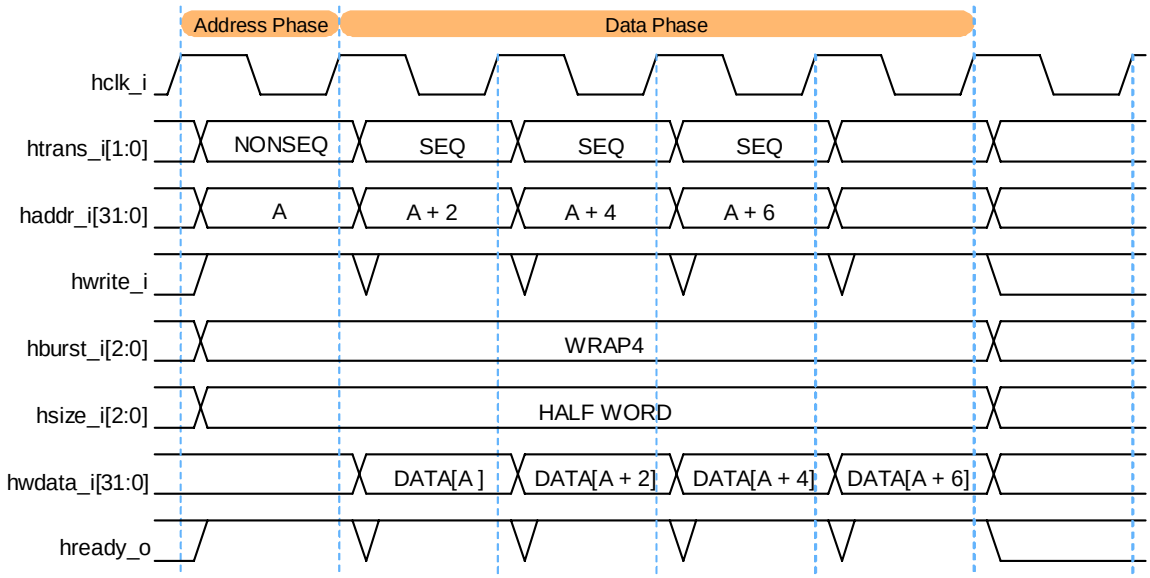

Figure 6: AHB Slave Burst Write Cycle Timing Diagram

5.1.4 Burst Read Cycle

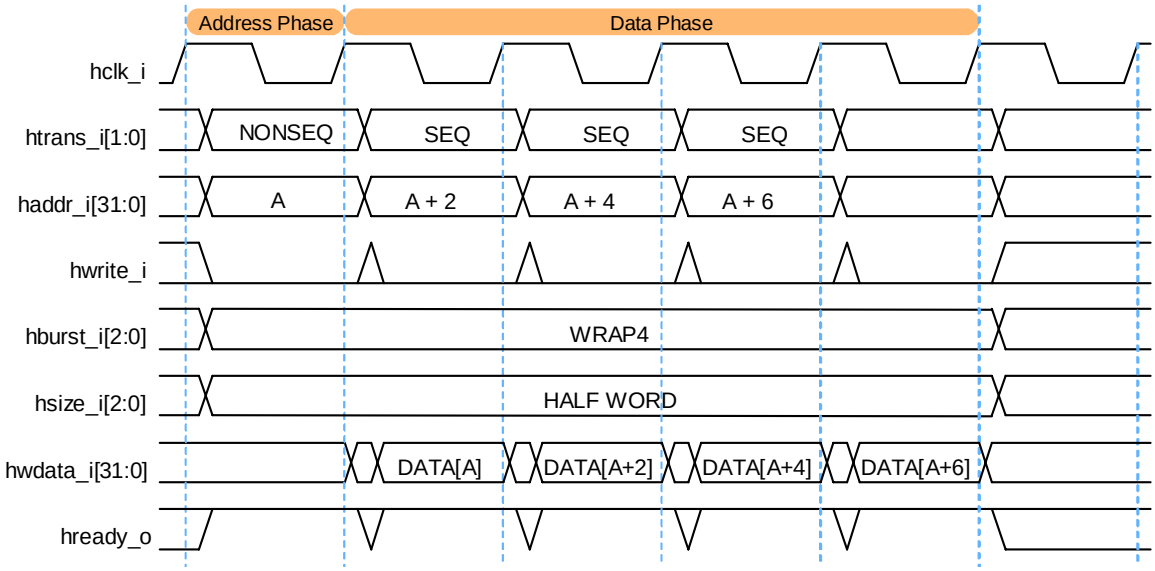

Figure 7: AHB Slave Burst Read Cycle Timing Diagram